REMARKS

Claims 1 and 69-84 are pending in the present application.

Claim 1 was amended.

Claims 69-84 have been added. Reconsideration of the claims is respectfully requested.

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at ***dvenglarik@novakov.com***.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

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APPENDIX A

1. (Amended) A method of forming a portion of a semiconductor integrated circuit, comprising:

forming a field oxide having an opening therethrough with substantially vertical sidewalls to an upper surface of a substrate underlying the field oxide, wherein the opening defines an active area;

forming a gate electrode over the surface of the substrate in the active area;

forming source and drain regions each including

a first portion in the substrate in the active area and

a second portion over the substrate adjacent above the first portion;

forming insulating regions between the gate electrode and the surface of the substrate in the active area and between the gate electrode and each of the second portions of the source and drain regions.

69. A method of forming a portion of a semiconductor integrated circuit, comprising:

forming a field oxide over a substrate, the field oxide having an opening therethrough to a surface of the substrate;

forming a gate electrode over the surface of the substrate and within the opening, the gate electrode having insulating material on a bottom and on two sides of the gate electrode, wherein the insulating material on the bottom of the gate electrode contacts the substrate; and

forming source and drain regions, each source and drain region including

a first portion in the substrate and

a second portion on the substrate over the first portion and adjacent to the insulating material on the sides of the gate electrode.

70. The method of claim 69, wherein the step of forming a field oxide over a substrate further comprises:

forming the opening through the substrate with substantially vertical sidewalls.

71. The method of claim 70, wherein the step of forming source and drain regions further comprises:

forming each source and drain region between a sidewall of the opening and the insulating material on the sides of the gate electrode.

72. The method of claim 71, wherein the step of forming source and drain regions further comprises:

filling a space between a sidewall of the opening and the insulating material on the sides of the gate electrode with material forming the second portion of one of the source and drain regions.

73. The method of claim 69, wherein the step of forming source and drain regions further comprises:

forming LDD regions for the source and regions within the first portion of each source and drain region.

74. The method of claim 73, wherein the step of forming LDD regions for the source and regions within the first portion of each source and drain region further comprises:

forming the LDD regions in the substrate beneath the insulating material on the sides of the gate electrode.

75. The method of claim 69, further comprising:

forming the gate electrode, the insulating material on the sides of the gate electrode, and the second portions of the source and drain regions to fill the opening.

76. The method of claim 69, further comprising:

forming the gate electrode with an upper surface further from a surface of the substrate than an upper surface of the field oxide.

77. An integrated circuit structure, comprising:

a substrate;

a field oxide over the substrate, the field oxide having an opening therethrough to a surface of the substrate;

a gate electrode over the surface of the substrate and within the opening, the gate electrode having insulating material on a bottom and on two sides of the gate electrode, wherein the insulating material on the bottom of the gate electrode contacts the substrate; and

source and drain regions adjacent the insulating material on the gate electrode, each source and drain region including

a first portion in the substrate and

a second portion on the substrate over the first portion and adjacent to the insulating material on the sides of the gate electrode.

78. The integrated circuit structure of claim 77, wherein the opening through the substrate has substantially vertical sidewalls.

79. The integrated circuit structure of claim 78, wherein each source and drain region is formed between a sidewall of the opening and the insulating material on the sides of the gate electrode.

80. The integrated circuit structure of claim 79, wherein a space between a sidewall of the opening and the insulating material on the sides of the gate electrode is filled with material forming the second portion of one of the source and drain regions.

81. The integrated circuit structure of claim 77, further comprising:
LDD regions for the source and regions formed within the first portion of each source and drain region.

82. The integrated circuit structure of claim 81, wherein the LDD regions are formed in the substrate beneath the insulating material on the sides of the gate electrode.

83. The integrated circuit structure of claim 77, wherein the gate electrode, the insulating material on the sides of the gate electrode, and the second portions of the source and drain regions fill the opening.

84. The integrated circuit structure of claim 77, an upper surface of the gate electrode is further from a surface of the substrate than an upper surface of the field oxide.